

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE  
**10/591193**

Appl. No. : Unassigned Confirmation No. Unassigned  
First Inventor : AZIMANE, Mohamed IAP5 Rec'd PCT/PTO 30 AUG 2006  
Filed : Concurrently  
TC/A.U. : Unassigned  
Examiner : Unassigned  
  
Docket No. : US04 0145 US3  
Customer No. : 24738  
  
Title: DFT Technique for Stressing Self-Timed Semiconductor  
Memories to Detect Delay Faults

Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

**PRELIMINARY AMENDMENT**

Sir:

Prior to calculation of the filing fee and examination please amend the above-identified application as follows:

**Amendments to the Specification** begin on page 2 of this paper.

**Amendments to the Claims** begin on page 3 of this paper.

**Remarks/Arguments** begin on page 4 of this paper.